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THE GROWTH OF EXPITAXIAL GaAs AND

GaAlAs ON SILICON SUBSTRATES BY OMVPE

8TH QUARTERLY REPORT ✓

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1.   INTRODUCTION

1.1   PLANNED WORK FOR QUARTER 8

The work programme for this quarter was as follows:-

(i)   Growth experiments to establish the dopant concentrations needed to meet the active and contact layer specifications of both GaAs/GaAs and GaAs/Si FETs.

(ii)   Growth of GaAs/Si and GaAs/GaAs FET structures.

(iii)   Processing and comparison of GaAs/GaAs and GaAs/Si FETs.

(iv)   Investigation of low temperature techniques for silicon surface preparation.

(v)   Investigation of dislocation filtering structures containing strained layer superlattices (SLS) consisting of alternating layers of different elastic constants.

(vi)   Further defect etching experiments and correlation with transmission electron microscopy (TEM) results.

1.2   SUMMARY OF PROGRESS IN QUARTER 8

Progress against these tasks is summarised below, and presented in detail in the subsequent sections of this report.

(i)   Growth experiments to establish the dopant concentrations needed to meet the active and contact layer specifications of both GaAs/GaAs and GaAs/Si FETs.

Appropriate adjustments have been made to accommodate the difference in selenium dopant incorporation between GaAs on GaAs, and GaAs on silicon, reported in quarter 7.

(ii) Growth of GaAs/Si and GaAs/GaAs FET structures

FET structures have been grown on semi-insulating gallium arsenide substrates, and on high-resistivity silicon substrates using a two stage growth technique. In both cases high resistivity GaAs FET buffer layers were grown without the need to adjust the V/III ratio during growth. Carrier densities down to $5 \times 10^{13} cm^{-3}$ were achieved by reducing selenium memory effects in the reactor, and by the use of adduct purified TMG.

(iii) Processing and comparison of GaAs/GaAs and GaAs/Si FETs

Two GaAs/GaAs and two GaAs/Si FET wafers have been prepared for processing. The GaAs/GaAs FETs which were processed first, passed the normal mesa isolation test $<10\mu A$ @ 40V over $20\mu m$ and have been processed as far as D.C. characterisation.

(iv) Investigation of low temperature techniques for silicon surface preparation

During the quarter a low pressure OMVPE system has been used for low temperature silicon surface preparation experiments. Epitaxial GaAs on silicon has been grown in this system on substrates which were cleaned by heating to temperatures of $900^{\circ}C$.

(v)   Investigation of dislocation filtering structures containing SLS consisting of alternating layers of different elastic constants.

All of the FET structures were grown using the "standard" dislocation filtering structure, 2 x 10 period $Ga_{0.85}In_{0.15}As/GaAs$ SLS with a 3000A GaAs spacer layer between them.

No further experimental dislocation filtering structures using either GaInAs/GaAs or GaAsP/GaAs have been grown. However, further investigation of the growth of GaAs on profiled silicon substrates showed a reduction in defect density from 10^8 to $10^7 cm^{-2}$ in the region of raised features on the silicon surface. These results imply that this approach could lead to more significant reduction of defect density.

(vi) Theoretical studies of dislocation filtering systems.

We have carried out further theoretical investigation of the effect of the interaction between dislocations in dislocation filtering structures. This data is presented in section 3.2.

(vii) Further defect etching experiments and correlation with TEM results.

Cathodo luminescence (CL) studies of GaAs on silicon have been carried out, which showed order of magnitude changes in CL peak positions which were related to tensile strain in the region of thermal expansion mismatch cracks. CL profiles through the layer have also been obtained. This work will be reported fully in Quarter 9.

2. MATERIALS GROWTH

2.1 DOPING OF GALLIUM ARSENIDE FOR FETs

As reported in quarter 7, doping levels for GaAs/Si were found to be a factor of 2 higher than those obtained in equivalent lower epitaxial growths for selenium doping in the range 10^{17} to mid 10^{18}. This difference was thought to be due to enhanced dopant incorporation via the defects in GaAs/Si. The OMVPE reactor was modified to give a wider doping range by using two sources of hydrogen selenide, both sources have been calibrated over their full range for the growth of both GaAs/GaAs and GaAs/Si. The factor of 2 difference in doping level for a given hydrogen selenide mole fraction, reported in quarter 7 was confirmed. The relation between hydrogen selenide mole fraction and doping level for GaAs/GaAs and for GaAs/Si grown under identical growth conditions is shown in figure 1.

In addition, selenium was found to exhibit a run-to-run memory effect, giving a background doping level of $>10^{15}cm^{-3}$ in an undoped layer grown in the run following the growth of a selenium doped layer. This problem was particularly significant in the case of FET structures where the last layer to be grown was the contact layer which was selenium doped to $2x10^{18}cm^{-3}$, followed by growth of the high resistance buffer layer in the next FET growth run. The problem was circumvented by the deposition of 3 μm of undoped GaAs in a separate growth run, to precondition the susceptor and reactor walls, prior to the growth of an FET.

2.2   GROWTH OF FET STRUCTURES

As agreed with the sponsor the major materials effort this quarter has been devoted to the growth of well characterised FET structures on both GaAs and Si substrates.

A number of FET layers have been grown to the GAT4 specification on semi-insulating gallium arsenide substrates, and on high-resistivity silicon substrates using a two stage growth technique.

An initial GaAs "base layer" structure consisting of the 400°C initialisation layer, the 20 min. thermal anneal at 750°C, and the GaInAs/GaAs SLS was grown on the silicon substrate which had been thermally cleaned at 1100°C.

In a second growth run the FET buffer, active and contact layers were then grown on this base layer, using exactly the same conditions as those used for homoepitaxial FETs.

Carrier concentrations of nominally undoped GaAs deposited on semi insulating GaAs substrates were in the region of $5 \times 10^{13}cm^{-3}$, with corresponding 77K mobilities in excess of $100,000cm^2V^{-1}s^{-1}$. This improvement in purity of undoped material was believed to be associated with the use of adduct purified TMG.

FET structures were grown on both GaAs and silicon/GaAs base layers using the adduct purified TMG source. These FET wafers were assessed by mercury probe

CV etch profiling, Fig. 2. This material is now being processed into GAT 4 FET devices.

2.3 GROWTH ON PROFILED SUBSTRATES

As previously reported (1), the use of exposed substrate edges to provide sites for "turned over" dislocations has been investigated. A reactive ion etched tungsten mask was used to allow wet etching of the silicon substrate using an $HF/HNO_3/H_2O$ mixture to form striped bars $1.3\mu m$-$1.6\mu m$ high and $6.0\mu m$ to $95\mu m$ wide. These substrates were included in several GaAs on silicon growth runs together with conventional planar (100) silicon wafers.

Interference contrast optical microscopy showed that the morphology of the GaAs/Si structures grown over the bars was the same as that obtained on the material between the bars. It was noticed however that thin lines of morphological defects parallel to the bars were formed in the areas between bars on most of the growths (Fig. 3). Their spacing from the neighbouring bar was dependent on the width of the bar and was also asymmetric for each one.

Surface contours of the profiled substrates obtained from the Dektak surface profiling instrument indicated that the lines of defects occurred near the point where the substrate surface started to curve towards the shallow trenches formed by wet etching of the bars. These trenches had different widths for each bar width and each side of the bars, in the manner observed for the defects. Optical observation of cleaved cross sections of these layers revealed that the defects were pits of around 30-50% of the epitaxial layer thicknesses.

Growth on the profiled substrate showed generally poor morphology except upon the bars and within a distance from each bar corresponding to the shallow trench regions (Fig. 4). The cause of this effect is not apparent, but may relate to problems with the etching behaviour of this particular substrate

Plan view TEM was used to calculate defect densities in these specimens. The defect density was studied as a function of the mean distance of any

particular area of growth from the nearest bar edge. Figures 5 and 6 show typical electron micrographs of 7µm and 95µm wide bars respectively, and demonstrate the edge effects observed, with dislocation denuded regions near each bar edge. Detailed results for OA 542 are shown in Figure 7. Although there is considerable scatter in the data, the trend is clearly that substantial dislocation density reductions can be obtained by substrate profiling.

Further substrates are being patterned by direct etching of the silicon wafers using a photo resist mask, in order to produce bars of 0.5µm-5.0µm width, with vertical edges and reduced trenching. Growth runs will be undertaken when these substrates become available.

2.4 LOW TEMPERATURE SILICON SURFACE CLEANING EXPERIMENTS

Introduction

Low temperature (<900°C) silicon substrate cleaning is essential for GaAs on silicon integration which necessitates the deposition of GaAs on processed silicon wafers.

The experiments described below were carried out using an OMVPE system not previously used for GaAs on Si, which had the option of low pressure growth, and had been constructed for mainly experimental growth studies.

The reasons for using this system for these experiments were as follows:-

The low pressure option offers some advantages for low temperature cleaning in that volatile surface contaminants may be removed more readily than in an atmospheric pressure system (2). There is also the possibility of in-situ plasma etching.

The system had additional source channels available which enabled the reactor to be provided with gases suitable for surface conditioning or nucleation experiments, e.g. silane and germane.

Experiments

A series of silicon surface preparation experiments was undertaken, using different wet chemical etches, and a wide range of in-situ thermal cleaning conditions.

Prior to loading in the reactor the substrates were chemically cleaned by one of four different treatments: "RCA" etch (3), "Shiraki" (4) etch, HF dip, or HF dip/Nitric acid oxidation.

In each experiment a piece of silicon, which had received no chemical clean at all, was used as a control specimen.

Four substrate orientations were used, (100), (100) misoriented by 2' towards [110], (100) misoriented by 2^0 towards [011], and (211).

In-situ cleaning before growth was carried out at temperatures ranging from 850^0C to 1150^0C and at pressures of 1 to 100 Torr in palladium diffused hydrogen, or hydrogen/arsine mixtures.

Hydrogen/silane mixtures containing low concentrations of SiH_4, e.g. $4x10^{-5}$ mole fractions, were used in an attempt to enhance the removal of oxide from the silicon surface by the possible reduction of SiO_2 to SiO and subsequent evaporation of SiO .

Hydrogen silane mixtures containing higher concentrations of SiH_4, e.g. $7x10^{-4}$ mole fractions were used to deposit a freshly prepared epitaxial silicon surface on which the growth of GaAs was initiated.

Some preliminary cleaning experiments were also carried out using an RF stimulated hydrogen plasma.

Assessment of the effectiveness of the various cleaning treatments was not a straightforward task since to remove the specimen from the reactor would involve exposure to the atmosphere and recontamination of the silicon surface.

The easiest option was simply to assess the quality of the silicon surface preparation by growing GaAs on it, and then assessing the layer by optical microscopy, X-ray diffraction, plan view and cross sectional TEM, and Auger profiling.

GaAs was deposited using the normal two stage growth technique, in the manner which has been described by Akiyama et al (5), at a reactor pressure of 100 Torr, with V/III ratios of up to 500:1.

Results

These experiments are at an early stage and are ongoing. So far the following results have been obtained:-

(1)   GaAs with X-ray rocking curves of FWHM = 173 arc secs has been grown on silicon substrates which were cleaned by heating to $900^{\circ}C$ in hydrogen at 100 Torr. Fig. 8.

(2)   The best surface morphologies, as revealed by interference microscopy, were obtained on those specimens which had received "RCA" or "Shiraki" type chemical treatments (3)(4). Fig. 9.

(3)   Auger analysis profiles through these structures showed the presence of oxygen at the silicon/GaAs interface. Fig. 10.

(4)   Stacking faults were observed in epitaxial silicon on silicon grown in this system, which was also an indication of the presence of oxygen or C on the Si surface. Fig. 11.

Further improvement in the quality of epitaxial growth is being sought by reduction of background water vapour/oxygen concentration in the reactor. Clearly the presence of any water vapour or oxygen in the system would compromise meaningful assessment of any low temperature cleaning experiments.

3.   MATERIALS ASSESSMENT

3.1   DISLOCATION THEORY

In previous Quarterly Reports [6], it has been demonstrated that knowledge of
the critical thickness of a strained layer is vital for the growth of defect
free layers. For GaAs-on-Si applications, strained layers are used as
"dislocation filters" which turn over threading dislocations to form misfit
dislocations, and such layers are required to be thicker than the critical
thickness for the formation of misfit dislocations, but must be thinner than
the critical thickness for the nucleation of additional threading dislocat-
ions. Calculations of these critical thicknesses (based on the equilibrium
models of Matthews and Blakeslee [7])were presented in Quarterly Report No. 6
[6] for InGaAs layers on GaAs. Unfortunately, however, the equilibrium
models used do not take into account dislocation-dislocation interactions,
which can be important if the interaction energy is comparable to the elastic
energy associated with the excess stress of the strained layer. Also,
dislocation-dislocation interactions can cause misfit dislocations to "bend
back" into the upper GaAs layers, somewhat defeating the object of using
strained layers. Dodson [8] has recently proposed a simple model aimed at
estimating the effects of dislocation-dislocation interactions on critical
thicknesses, and, although only interactions between parallel misfit
dislocations are included, he claims to obtain good agreement with experiment
for the degree of strain relaxation in buffer layers (which does not agree
with predictions from the equilibrium models).

Dislocation-dislocation interactions also occur for perpendicular misfit
dislocations, and can lead to misfit dislocation multiplication by the
Hagen-Strunk mechanism [9].

In this reporting period, attempts have been made to estimate the importance
of dislocation-dislocation interactions. Blin's formula [10] for the
interaction energy between two arbitrarily shaped dislocation loops has been
used to evaluate the interaction energy between two misfit dislocations in
various configurations and with various Burgers vectors. Preliminary results
indicate that the interaction energy can be comparable to the energy of an
isolated dislocation for typical dislocation separations of interest here.

The implications of these results for critical thickness calculations are now being studied, and will be discussed in the next Quarterly report, along with a full report of the calculations based on Blin's formula [10].

4.   DEVICES

4.1   PROCESSING AND ASSESSMENT OF GaAs/Si MESFETs

Two GaAs/GaAs and two GaAs/Si FET wafers were prepared for processing, and assessment showed that they were all grown accurately to the GAT4 layer specification. The GaAs/GaAs FETs were processed first and showed good gate isolation, with an acceptable isolation breakdown of 40V for a 10μA current passing between mesas 20μm apart. Processing of these wafers is ongoing and results will be reported in the next quarterly report.

5.   CONCLUSIONS

(1)   Selenium incorporation in n-type GaAs on silicon is increased by a factor of two over equivalent doping in homoepitaxial GaAs for the full range of n-type doping required for FET structures. (1×10^{17} to $2 \times 10^{18} cm^{-3}$).

(2)   High resistance GaAs layers, suitable for FET buffer layers, can be grown by OMCVD using a high purity TMG source without the need to adjust the V/III ratio during growth.

(3)   The effect of autodoping occurring during the high temperature thermal clean of the silicon substrate can be circumvented by using a two stage growth procedure.

(4)   Selenium is found to have a run-to-run memory effect, giving a background doping level of $>10^{15} cm^{-3}$ in an undoped layer grown in the run following the growth of a selenium doped layer. This memory effect can be overcome by the growth of a nominally undoped GaAs susceptor conditioning layer prior to the growth of an FET buffer layer.

(5)   Preliminary res·lts from the low temperature cleaning experiments are encouraging, and suggest that low temperature cleaning schedules can be developed when the low pressure system integrity is improved.

(6)   Growth on profiled substrates can lead to significant reduction in dislocation density, by at least one order of magnitude.

6.   PLANNED WORK FOR QUARTER 9

(1)   Growth of GaAs on Si FETs and GaAs/GaAs control specimens.

(2)   Processing, assessment and testing of discrete devices fabricated from the material grown in (1).

(3)   Continue experimental growths of GaAs on profiled silicon substrates.

(4)   Continue low temperature substrate preparation experiments.

(5)   Selective area epitaxy of GaAs on silicon.

(6)   Defect reducing experiments using repetitive anneal-grow sequences.

(7)   Use of SLS in conjunction with (7).

7.   REFERENCES

[1]   Quarterly report No. 4 (June-August 1987).

[2]   Ghidini and Smith, J. Elec. Chem. Soc., Vol. 131, No. 12, Dec. 84, pp.2924-2928.

[3]   Werner Kern and David A Puotinen. RCA Review June 1970.

[4]   Akitoshi Ishigaka and Yasuhiro Shiraki
      J. Electrochem Soc., Vol. 133, No. 4, April 1986, pp.666-671.

[5]   Akiyama et al, Mat. Res. Symp. Proc. Vol. 67, 1986, pp.53-64.

[6]   Quarterly Report No. 6 (December 87 - February 88).

[7]   J W Matthews, A E Blakeslee, S Mader
      Thin Solid Films, 33 (1976), pp.253-266.

[8]   B W Dodson, Appl. Phys. Lett., 53 (1988), pp.37-38.

[9]   W Haghen, H Strunk, Appl. Phys. 17 (1978), pp.85-87.

[10] J P Hirth, J Lothe, "Theory of Dislocations", (Wiley, 1982).

8.   <u>FIGURES</u>

(1)   Hydrogen selenide doping calibration GaAs/GaAs cf. GaAs/Si.

(2)   Mercury probe CV profiles of GaAs/GaAs and GaAs/Si FETs.

(3)   Optical micrograph of surface of material on patterned substrate.

(4)   Optical micrograph of surface of material on patterned substrate.

(5)   TEM micrograph of dislocatons in $7\mu m$ wide bar.

(6)   TEM micrograph of centre of $\sim 100\mu m$ wide bar.

(7)   TEM micrograph dislocation densities of patterned areas versus distance to dislocation sink.

(8)   X ray rocking curve of GaAs/Si grown on substrate cleaned at $900^{\circ}C$.

(9)   Surface morphology of GaAs on chemically etched substrate.

(10)   Auger profile showing oxygen at interface between GaAs and silicon.

(11)   Stacking faults in epitaxial silicon on silicon grown in LP OMVPE system.
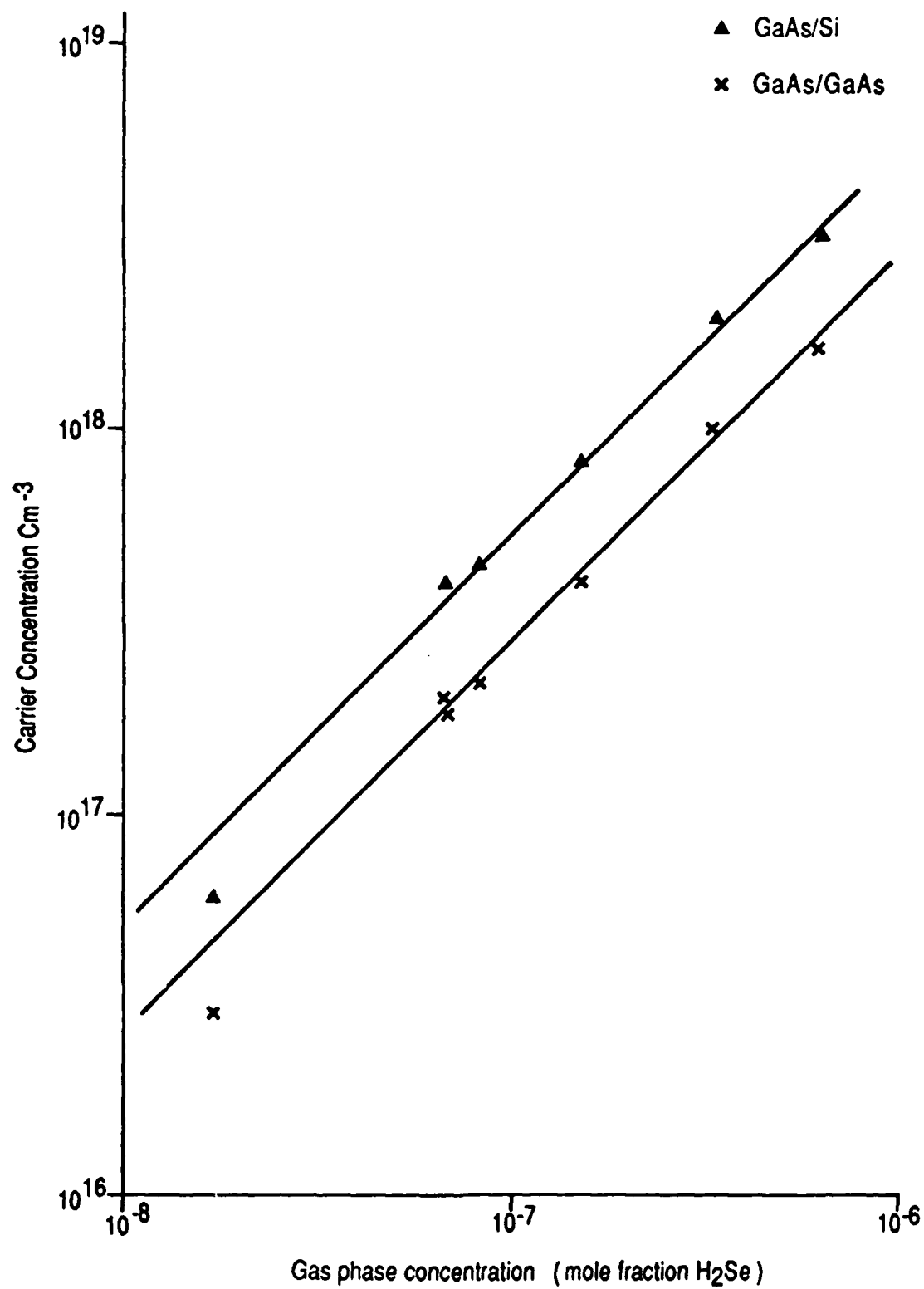
Fig. 1   Selenium doping calibration for GaAs on GaAs and GaAs on Silicon

GaAs / GaAs FET

GaAs / Si FET

OA - 652

OA - 653

OA - 657

OA - 664
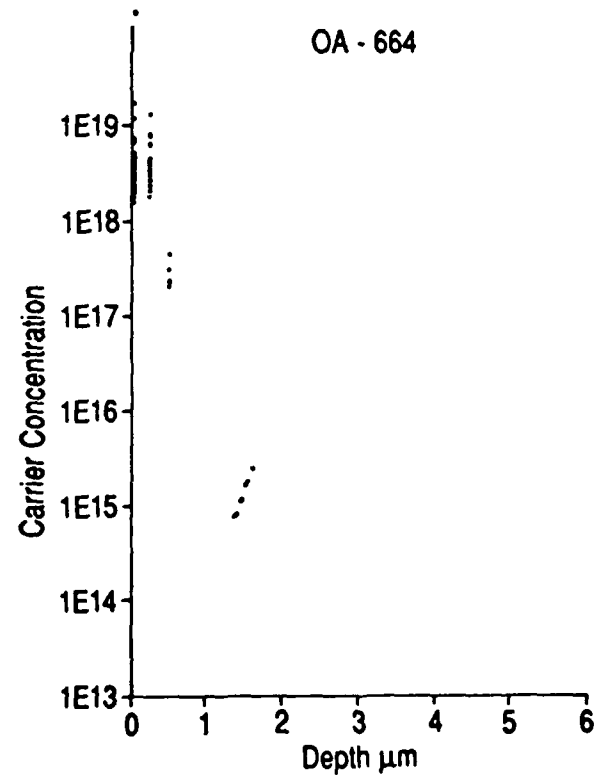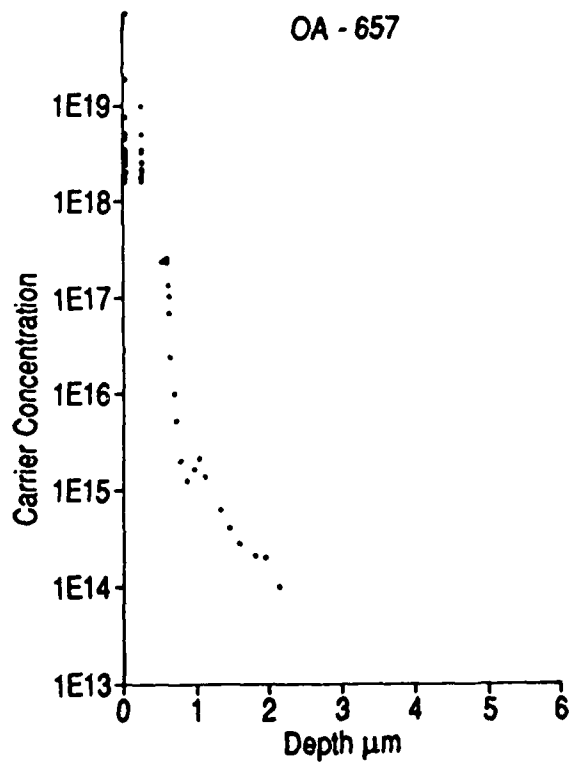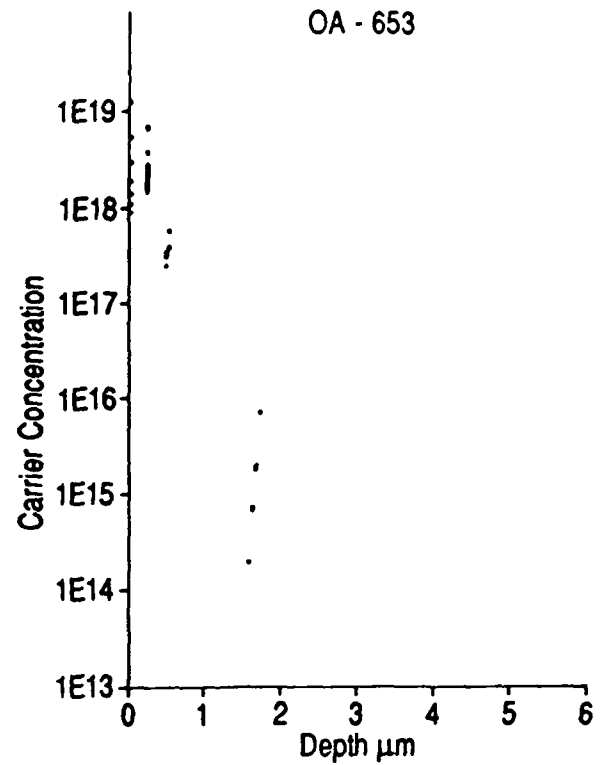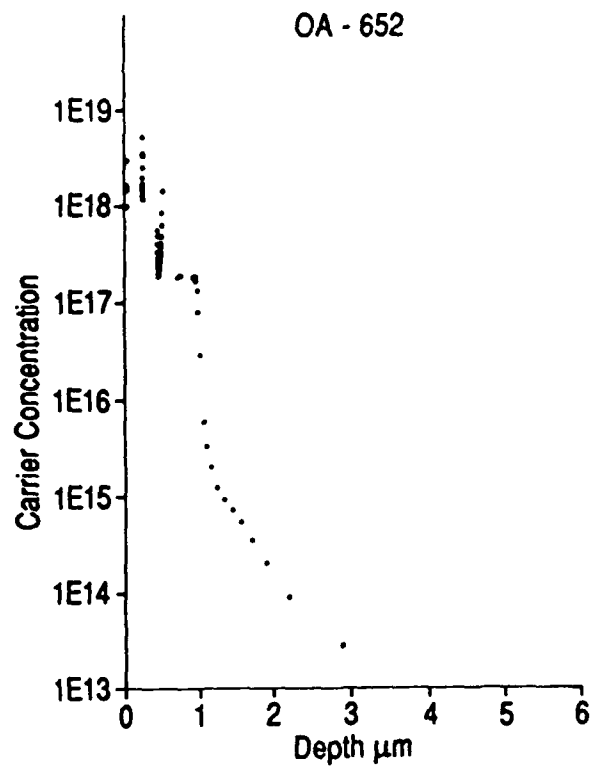
Fig. 2   Mercury probe CV profiles of FETs on Si and GaAs substrates

x40

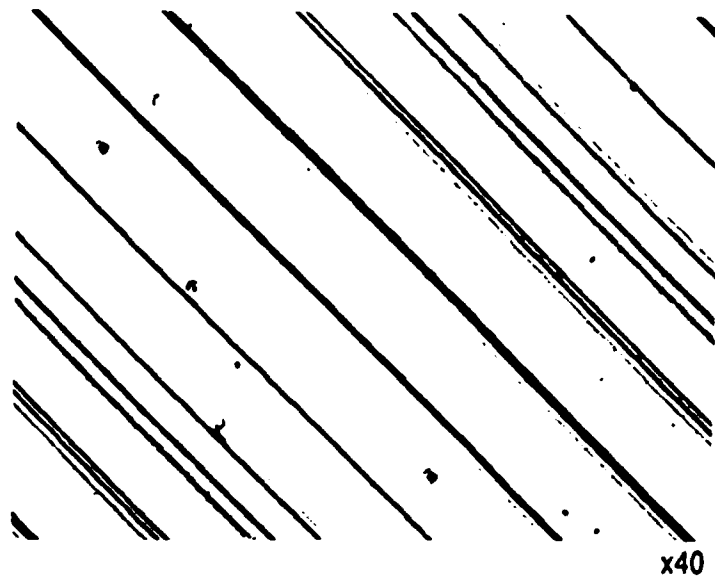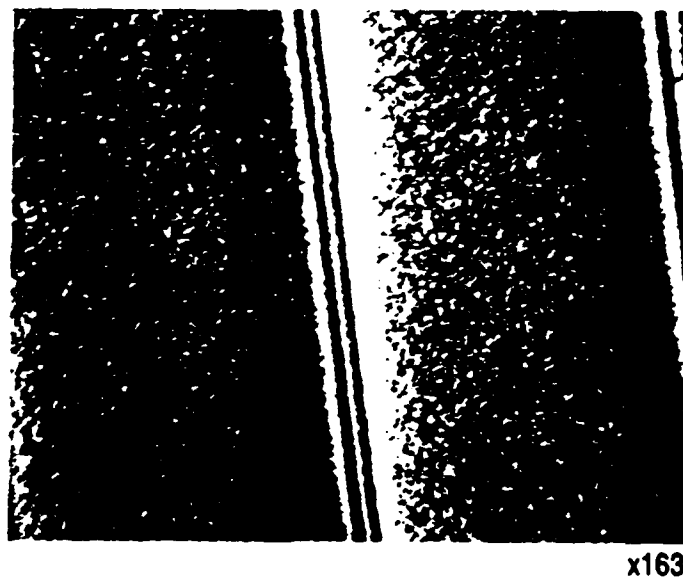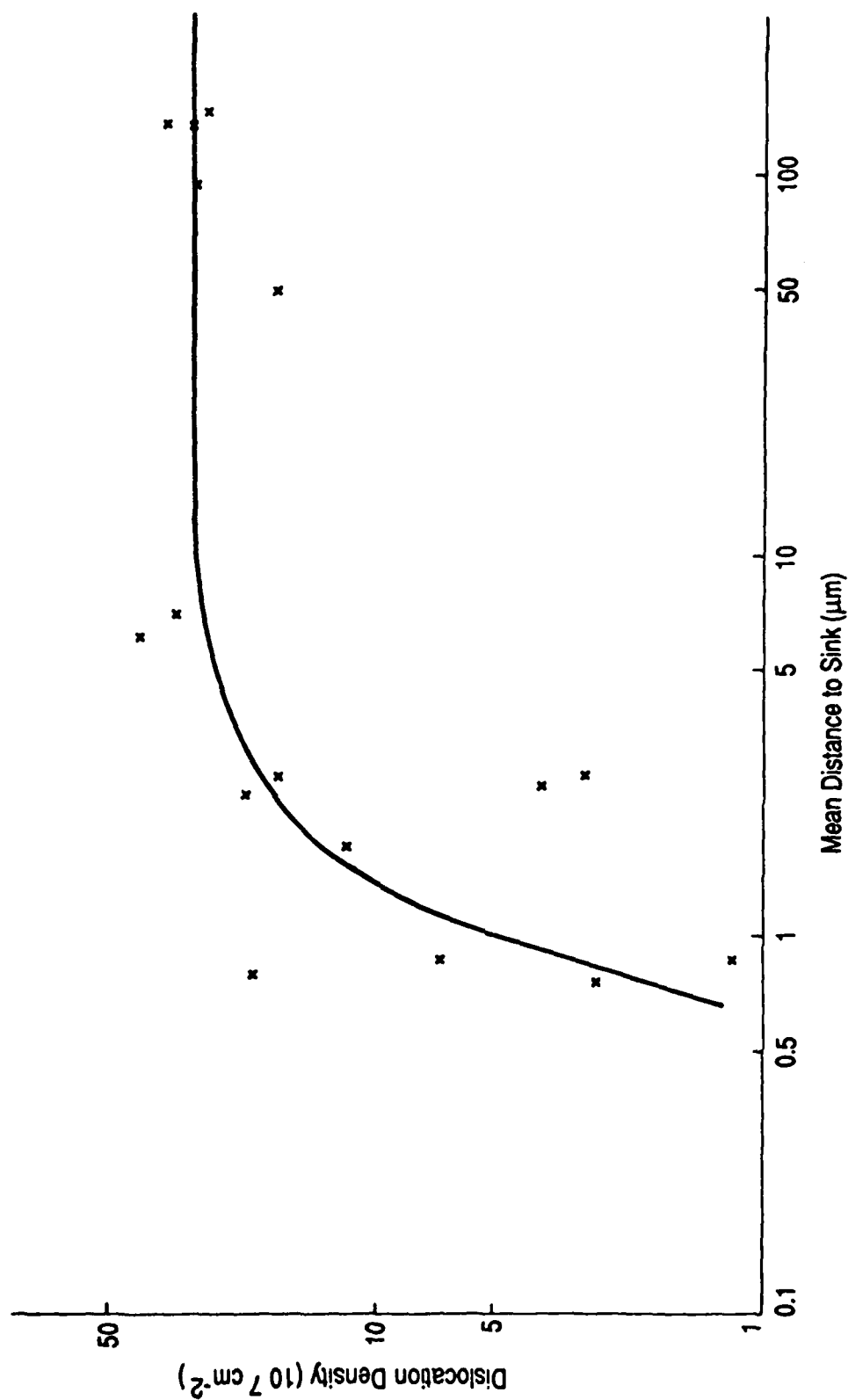Fig. 3   Optical micrograph of surface of GaAs on patterened substrate

x163

Fig. 4   Optical micrograph of surface of GaAs on patterened substrate

g_{220}

1.2μm

Fig. 5. TEM Micrograph of dislocations in 7μm wide bar

1.2μm

Fig. 6   TEM Micrograph of centre of ~ 100μm wide bar

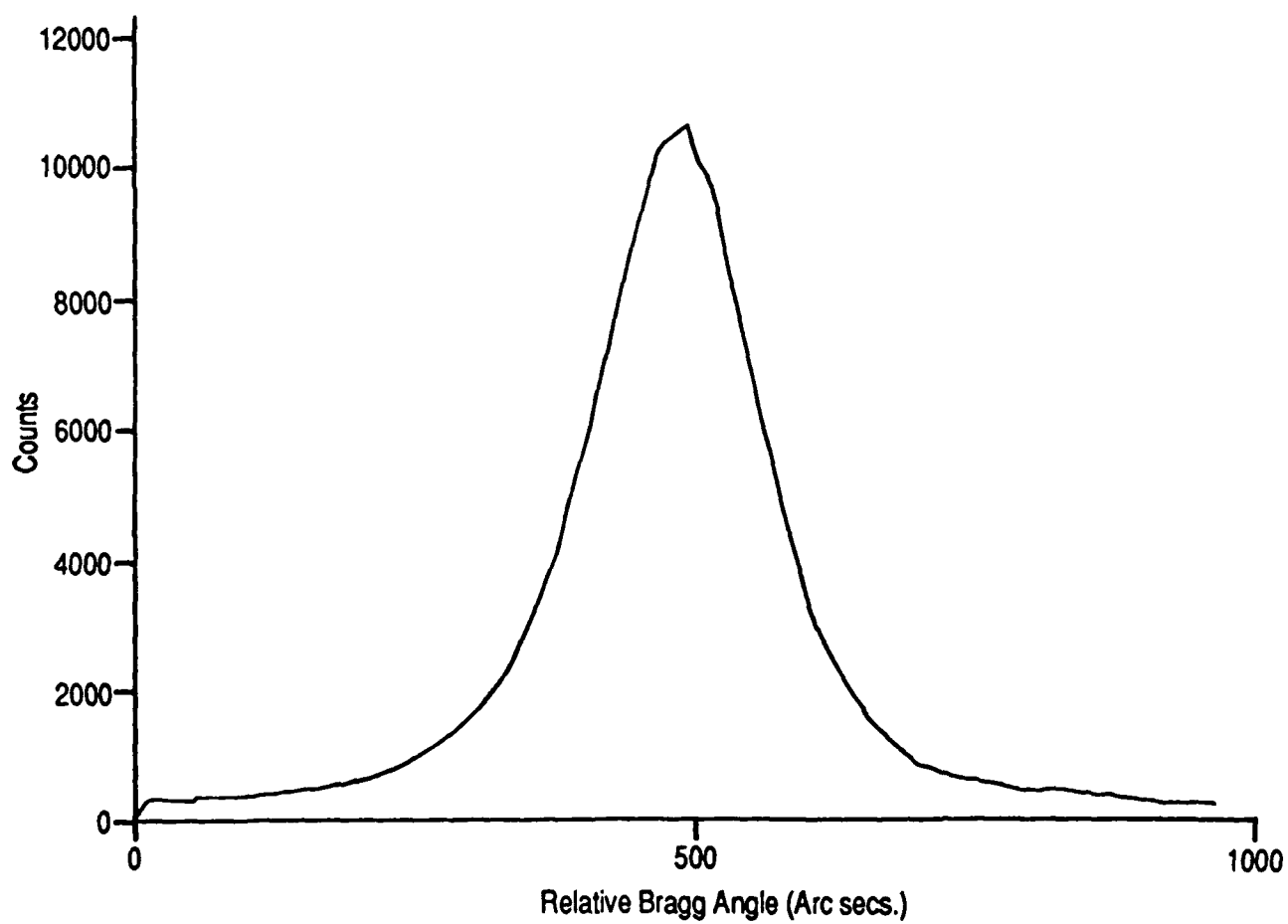Fig. 7 TEM Micrograph dislocation densities of pattered areas of OA 542 versus distance to dislocation sink.
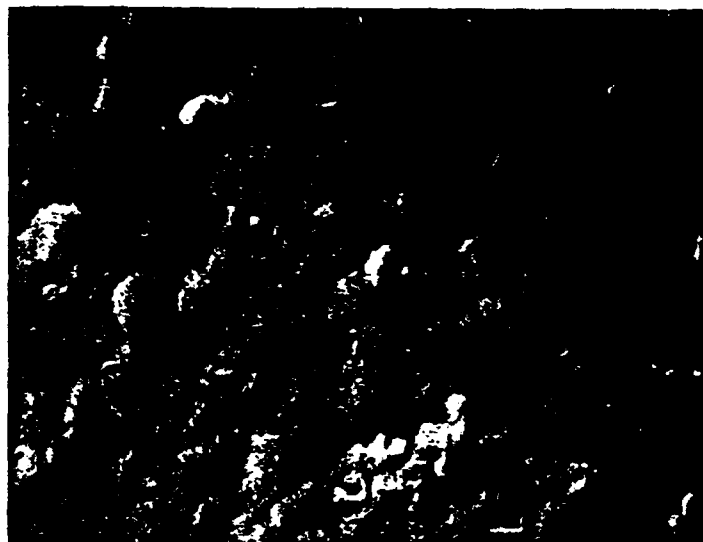
Fig. 8 X-ray rocking curve of GaAs on Silicon cleaned at 900°C. FWHM = 173 Arc secs.

10μm

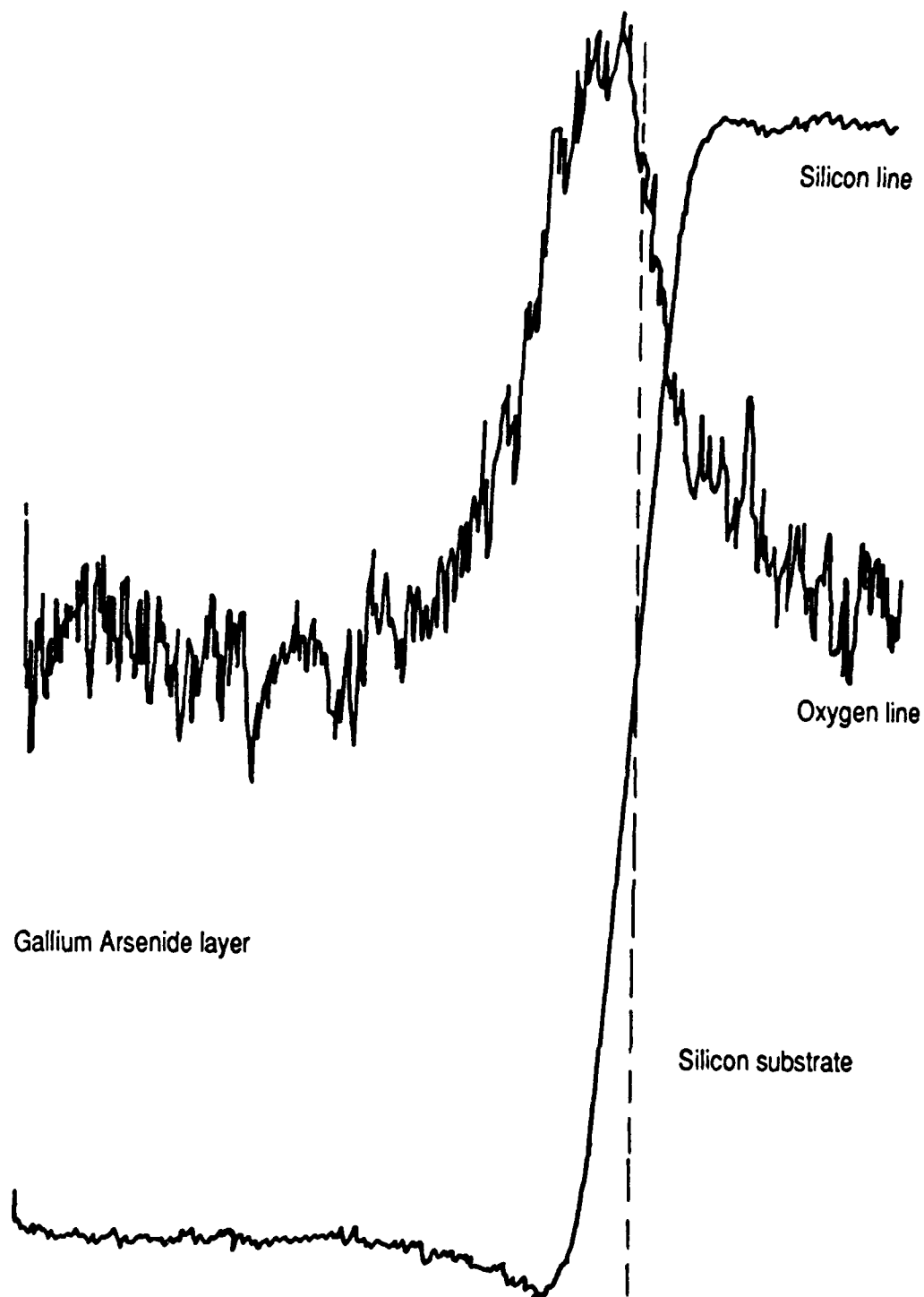Fig. 9   Surface morphology of GaAs grown on silicon cleaned at 900°C.

Silicon line

Oxygen line

Gallium Arsenide layer

Silicon substrate
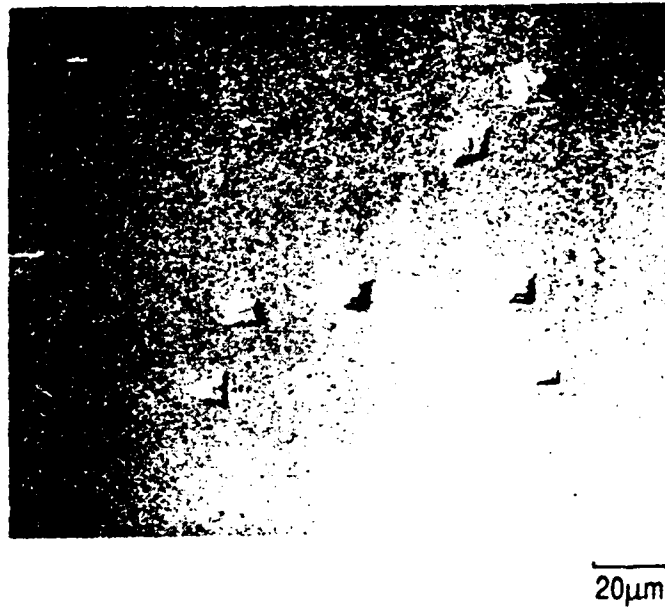
Fig. 10 AES Profile showing oxygen at interface.

20μm

Fig. 11   Stacking faults in silicon on silicon layers.